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April 26, 2002

To: Commissioner of Patents and Trademarks  
Washington, D.C. 20231

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TECHNOLOGY CENTER 2806

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Subject:

Serial No. 10/083,991 02/26/02

Chia-Der Chang et al.

PLANARIZATION METHOD FOR DEEP SUB  
MICRON SHALLOW TRENCH ISOLATION  
PROCESS

Grp. Art Unit: 2812

#### INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56. Copies of each document is included herewith.

#### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being  
deposited with the United States Postal Service as first class  
mail in an envelope addressed to: Commissioner of Patents and  
Trademarks, Washington, D.C. 20231, on April 29, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

SB Ackerman 4/29/02

U.S. Patent 6,180,525 to Morgan, "Method of Minimizing Repetitive Chemical-Mechanical Polishing Scratch Marks and of Processing a Semiconductor Wafer Outer Surface," describes a method of minimizing repetitive chemical mechanical polishing scratch marks.

U.S. Patent 5,728,621 to Zheng et al., "Method for Shallow Trench Isolation," describes a method of planarizing a high quality oxide used in shallow trench isolation.

U.S. Patent 6,037,251 to Tu et al., "Process for Intermetal SOG/SOP Dielectric Planarization," describes a method for planarizing spin-on-glass used for intermetal insulation.

U.S. Patent 6,270,353 to Andrews et al., "Low Cost Shallow Trench Isolation Using Non-Conformal Dielectric Material," describes a method for planarizing a structure such as a shallow trench isolation region.

U.S. Patent 6,114,220 to Tsai, "Method of Fabricating a Shallow Trench Isolation," describes a method of fabricating a shallow trench isolation including the formation of a trench in a substrate.

Sincerely,



Stephen B. Ackerman, Reg. #37761